

PAT-NO: JP356140722A  
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TITLE: NOISE ELIMINATING CIRCUIT  
PUBN-DATE: November 4, 1981

INVENTOR-INFORMATION:  
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N/A

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ABSTRACT:

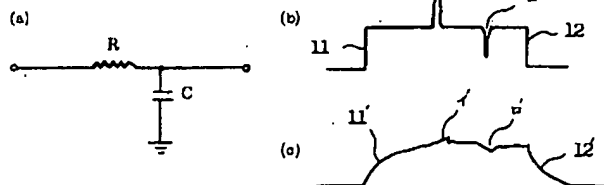
PURPOSE: To eliminate the noise in accordance with the variation of the noise width and without using any analog process, by comparing the past transmission signal stored temporarily with the present transmission signal to decide whether the signal inversion is due to the noise or not.

CONSTITUTION: The delayed flip-flop 4 stores temporarily the input signal 1 with the next clock pulse and then applies the output 4' to the state comparison logic circuit 6. The circuit 6 compares the input signal 1 during the one-preceding clock with the present input signal 1 in terms of the state and then applies the signals 7' and 8' contrary to each other to the next stage, and then shifts the waveform inverted by the noise at and

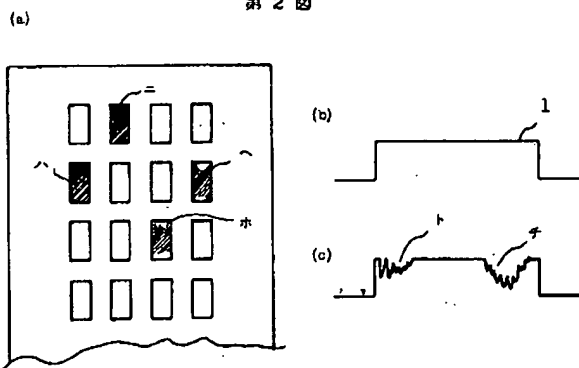
after the  
breaking point of the clock pulse to apply it to the delayed flip-  
flop 5. The  
flip-flop 5 supplies the arithmetic result signal 9' synchronously  
with the  
next clock pulse 2 and accordingly eliminates the noise equivalent to  
one clock  
pulse. Then the input signal is restored and the output signal 3 is  
supplied.

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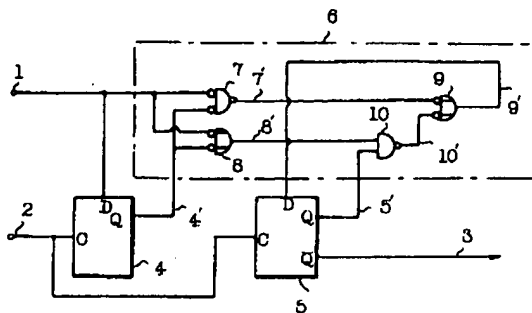
第1図



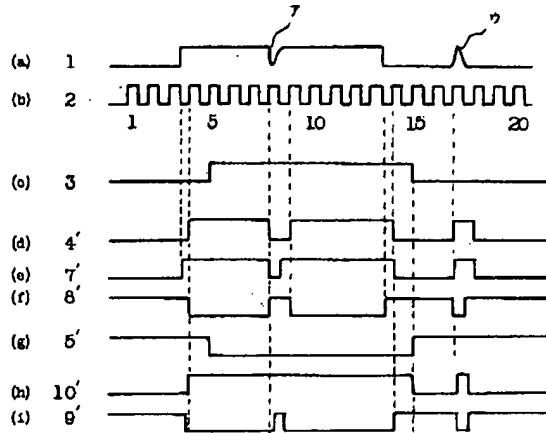
第2図



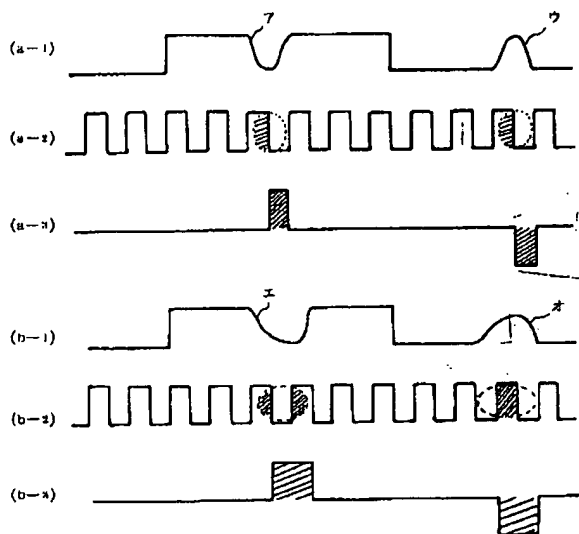
第3図



第4図



第5図



第6図

